AMENDMENTS TO THE CLAIMS

Please amend the claims follows:

1. (Currently Amended) A communication device, comprising:

a signal modulator/demodulator(modem), ~~having a digital signal processor~~ for effecting radio communications, having an interface operatively connected to a packet bus having N data lines for conveying packetized control and data signals; and

an application processor (AP) having a central processing unit operatively connected to a processor bus including address lines and M data lines, wherein M is greater than N;

and a master controller, operatively connected to the processor bus and to the packet bus, for controlling via ~~a common~~the packet bus a plurality of peripherals operatively connected to the packet bus~~including an interface with the signal modulator/demodulator~~.

2. (Currently Amended) The device of claim 1, ~~wherein~~ further including a shared memory operatively connected to the modem and the master controller for access by either the modem or the central processing unit ~~a memory shared by the modem and the AP is controlled via the interface~~.

3. (Original) The device of claim 2, wherein the shared memory is an SDRAM.

4. (Currently Amended) The device of claim 1, wherein the plurality of peripherals operatively connected to the packet bus includes the modem and at least one of an image capture module, a display, and a flash memory.

5. (Currently Amended) The device of claim 1, wherein the master controller controls the plurality of peripherals by issuing a packetized command commonly receivable by the plurality of peripherals over the ~~common~~ packet bus, wherein the packetized command includes a module device select signal used for selecting one of the plurality of peripherals.

6. (Currently Amended) The device of claim 5, wherein the selected one of the plurality of peripherals returns a signal to the master controller to acknowledge receipt of the packetized command.

7. (Original) The device of claim 5, wherein the packetized command includes a read/write command to a memory shared by the modem and the AP.

8. (Original) The device of claim 7, wherein data read from the shared memory is sent to the AP with a strobe signal, the strobe signal is used for strobing the data read into a register in the master controller.

9. (Original) The device of claim 3, wherein the SDRAM includes a plurality of data banks and an interface for interfacing the master controller.

10. (Original) The device of claim 3, wherein the SDRAM includes a protection circuit for receiving address data from the AP and the modem and for generating a protect signal upon receiving the same address from the modem and the AP.

11. (Currently Amended) A communication device, comprising:

a signal modulator/demodulator, ~~having a digital signal processor~~ for effecting radio communications, having an interface operatively connected to a second packet bus having N data lines for conveying packetized control and data signals; and

~~an application processor (AP) having a~~ central processing unit operatively connected to a processor bus including address lines and M data lines, wherein M is greater than N; and

a master controller, operatively connected to the processor bus and to a first packet bus having N data lines and to the second packet bus, for controlling via ~~a~~ the first packet bus at least

one peripheral and via ~~a~~ the second packet bus a memory shared by the modem and by the central processing unit~~AP~~.

12. (Original) The device of claim 11, wherein the master controller further controls via the second bus a flash memory.

13. (Original) The device of claim 11, wherein the at least one peripheral is an image capture module.

14. (Currently Amended) The device of claim 11, wherein the master controller controls a plurality of peripherals operatively connected to first packet bus by issuing a packetized command commonly receivable by the plurality of peripherals over the ~~common~~ first packet bus, the packetized command includes a module device select signal used for selecting one of the peripherals.

15. (Currently Amended) The device of claim 14, wherein the selected one of the plurality of peripherals returns a signal to the master controller to acknowledge receipt of command.

16. (Currently Amended) The device of claim 14, wherein the packetized command includes a read/write command to the memory shared by the modem and the central processing unit~~AP~~.

17. (Original) The device of claim 16, wherein data read from the shared memory is sent to the master controller with a strobe signal, the strobe signal is used for strobing the data read into a register in the master controller.

18. (Original) The device of claim 11, wherein the shared memory is an SDRAM.

19. (Currently Amended) The device of claim 18, wherein the SDRAM includes a plurality of data banks and an interface for interfacing the master controller via the second packet bus.

20. (Currently Amended) The device of claim 18, wherein the SDRAM includes a protection circuit for receiving address data from the central processing unit ~~AP~~ and the modem via the second packet bus and for generating a protect signal upon simultaneously receiving the same address from the modem and the central processing unit~~AP~~.

21. (Currently Amended) An application processor (AP), for use in a communication device, ~~the application processor comprises~~comprising:

a central processing unit, operatively connected to a processor bus including address lines and M data lines, for processing data received from a plurality of peripherals including a signal modulator/demodulator (modem) for effecting radio communications; and

a master controller operatively connected to the processor bus and to a second bus having N data lines, for controlling via ~~a~~ the ~~common~~ second bus the plurality of peripherals ~~and for interfacing with a signal modulator/demodulator (modem) via the common bus~~, wherein M is greater than N.

22. (Currently Amended) The device of claim 21, further including a memory operatively connected to the second bus, the memory being shared by the modem and by the central processing unit~~AP~~.

23. (Original) The device of claim 22, wherein the shared memory is an SDRAM.

24. (Currently Amended) The device of claim 21, wherein the plurality of peripherals additionally includes at least one of an image capture module, a display, and a flash memory.

25. (Currently Amended) The device of claim 21, wherein the master controller controls the plurality of peripherals by issuing a packetized command commonly receivable by the plurality of peripherals over the common bus, wherein the packetized command includes a module device select signal used for selecting one of the peripherals.

26. (Original) The device of claim 25, wherein the selected one of the peripherals returns a signal to the master controller to acknowledge receipt of the packetized command.

27. (Currently Amended) The device of claim 25, wherein the packetized command includes a read/write command to ~~a~~ the memory shared by the modem and by the central processing unit~~AP~~.

28. (Currently Amended) The device of claim 27, wherein data read from the shared memory is sent to the central processing unit~~AP~~ with a strobe signal, the strobe signal is used for strobing the data read into a register in the master controller.

29. (Original) The device of claim 23, wherein the SDRAM includes a plurality of data banks and an interface for interfacing the master controller.

30. (Currently Amended) The device of claim 23, wherein the SDRAM includes a protection circuit for receiving address data from the central processing unit~~AP~~ and the modem and for generating a protect signal upon simultaneously receiving the same address from the modem and the central processing unit~~AP~~.

31. (Currently Amended) An application processor (AP) for use in a communication device, the application processor comprises:

a central processing unit, operatively connected to a processor bus including address lines and M data lines, for processing data received from a plurality of peripherals; and

a master controller operatively connected to the processor bus including address lines and to a first packet bus having N data lines and to a second packet bus, for controlling via ~~a~~ the first packet bus the plurality of peripherals, and for controlling~~interfacing with a~~ the signal modulator/demodulator (modem) via ~~a~~ the second packet bus.

32. (Currently Amended) The device of claim 31, further including a ~~memory, the~~ memory ~~being~~ shared by the modem and the central processing unit~~AP~~.

33. (Original) The device of claim 32, wherein the shared memory is an SDRAM.

34. (Currently Amended) The device of claim 31, wherein the plurality of peripherals operatively connected to the first packet bus include at least one of an image capture module, a display, and a flash memory.

35. (Currently Amended) The device of claim 31, wherein the master controller controls the plurality of peripherals by issuing a packetized command commonly receivable by the plurality of peripherals over the ~~common~~ first packet bus, the packetized command includes a module device select signal used for selecting one of the peripherals.

36. (Original) The device of claim 35, wherein the selected one of the peripherals returns a signal to the master controller to acknowledge receipt of the packetized command.

37. (Currently Amended) The device of claim 35, wherein the packetized command

includes a read/write command to a memory shared by the modem and the central processing unit~~AP~~.

38. (Currently Amended) The device of claim 37, wherein data read from the shared memory is sent to the central processing unit~~AP~~ with a strobe signal, the strobe signal is used for strobing the data read into a register in the master controller.

39. (Currently Amended) The device of claim 33, wherein the SDRAM includes a plurality of data banks and an interface for interfacing the master controller via the second packet bus.

40. (Currently Amended) A method of controlling a communication device having a signal modulator/demodulator (modem) for effecting radio communications and ~~an application processor (AP) having~~ a central processing unit, and a master controller, comprising:

controlling a master controller via a processor bus;

controlling ~~via a common bus in the master controller~~ a plurality of peripherals including the signal modulator/demodulator via a common bus operatively connected to the master controller and to each of the plurality of peripherals; ~~and~~

~~interfacing with the signal modulator/demodulator via the common bus~~.

41. (Currently Amended) The method of claim 40, wherein the step of ~~interfacing~~ controlling the signal modulator/demodulator includes interfacing a memory shared by the modem and the central processing unit~~AP~~.

42. (Original) The method of claim 40, wherein the shared memory is an SDRAM.

43. (Original) The method of claim 40, wherein the step of controlling includes

controlling at least one of an image capture module, a display, and a flash memory.

44. (Currently Amended) The method of claim 40, wherein the step of controlling the plurality of peripherals includes issuing a packetized command commonly receivable by the plurality of peripherals over the common bus, wherein the packetized command includes a module device select signal used for selecting one of the peripherals.

45. (Original) The method of claim 44, wherein the selected one of the peripherals returns a signal to the master controller to acknowledge receipt of the packetized command.

46. (Currently Amended) The method of claim 40, wherein the packetized command includes a read/write command to a memory shared by the modem and the central processing unit~~AP~~.

47. (Currently Amended) The method of claim 40, wherein data read from the shared memory is sent to the central processing unit~~AP~~ with a strobe signal, the strobe signal is used for strobing the data read into a register in the master controller.

48. (Currently Amended) The method of claim 41, further including receiving address data from the central processing unit ~~AP~~ and the modem at the shared memory and generating a protect signal upon simultaneously receiving the same address from the modem and the central processing unit ~~AP~~.